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REMARKS

Claims 1-4 and 10-12 are pending in the Application. Claims 1-4 and 10-12 are rejected under 35 U.S.C. § 103(a). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw all outstanding rejections.

I. REJECTIONS UNDER 35 U.S.C. § 103(a):

The Office Action has rejected claim 1 as being unpatentable over *Cappelletti et al.* (U.S. Patent No. 5,637,520) (hereinafter "*Cappelletti*") in view of *Nakata* (U.S. Patent No. 5,254,489). The Office Action has further rejected claims 2 and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Cappelletti* in view of *Nakata* in further view of *Lee* (U.S. Patent No. 5,175,120). The Office Action has further rejected claims 3-4 and 11-12 under 35 U.S.C. § 103(a) as being unpatentable over *Cappelletti* in view of *Nakata* and *Lee* and further in view of *Chien et al.* (U.S. Patent No. 6,436,759) (hereinafter "*Chien*").

A. *Chien* is not a prior art reference.

The Applicants respectfully submit that *Chien* is not a prior art reference because *Chien*'s filing date post dates the filing date of the present invention. The present invention is a divisional application of a parent application filed June 15, 2000. *Chien*'s filing date is January 19, 2001. Accordingly, *Chien* cannot be a prior art reference in the present invention. Therefore, the rejections to claims 3-4 and 11-12 are moot.

B. The Examiner has not provided any motivation for combining the references *Cappelletti*, *Nakata* and *Lee*.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The motivation or suggestion to

combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q. 2d. 1453,1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re Lee*, 277 F. 3d 1338, 1343, 61 U.S.P.Q. 2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F. 3d 1365, 1370, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q. 2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

In order to reject under 35 U.S.C. § 103, therefore, the Examiner must provide a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q. 2d 1453, 1457-1458 (Fed. Cir. 1998); MPEP § 2142. The Examiner's motivation for modifying *Cappelletti* for strengthening the interface by providing a nitrification process in both the core area and the periphery area of the memory device thereby improving the reliability of the dual gate oxide in the core area is "because the nitridation allows for a gate film of longer endurance." Paper No. 8, page 2. The Examiner's motivation for modifying *Cappelletti* to deposit a layer of type-1 polysilicon in both the core area and periphery area of the memory device, and to deposit a layer of oxide nitride oxide over the layer of type-1 polysilicon, and to remove the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device is "because this is shown to be conventional fabrication for memory and peripheral circuits." Paper No. 8, page 3.

1. <u>There is no motivation to combine *Cappelletti* with *Nakata*</u>

There's no motivation to combine *Cappelletti* with *Nakata* as there is no suggestion or motivation in either *Cappelletti* or *Nakata*, or in their combination, or in the knowledge of those ordinarily skilled in the art to combine the teaching of a method for producing a flash-EEPROM memory array and associated transistors using the DPCC process as taught in *Cappelletti* with the teaching of setting the thickness of a first gate oxide film independently of the thickness of the gate oxide film formed in a later thermal oxidation step as taught in *Nakata*. *Cappelletti* teaches:

> The process according to the present invention thus provides a method for *producing a flash-EEPROM memory array and associated transistors using the DPCC process*, and thus exploits the intrinsic advantages, and in particular the experience and know-how of the process for obtaining memories of known, reliable electric characteristics. Moreover, the possibility of producing flash-EEPROM memories using the DPCC process allows for the production of two families of products (EPROM and flash-EEPROM memories) on the same fabrication line with no significant differences, and by using the same machinery. Column 5, lines 1-11.

Thus, *Cappelletti* teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process. Further, *Nakata* teaches:

> According to this invention, there is provided a method of manufacturing a semiconductor device. An element region and an element isolation region are formed on a semiconductor substrate of a first conductivity type. A first oxide film prospectively serving as a gate insulating film is formed in the element region. Thermal oxidization is performed after annealing is performed in nitrogen or ammonia atmosphere to nitrify an entire surface of the first oxide film. A predetermined region of a nitrified first oxide film is removed, and a second oxide film prospectively serving as a gate insulating film is formed in the predetermined region using the nitrified first oxide film as a mask. A gate electrode constituted by a polysilicon film is formed on each of the nitrified first oxide film and the second oxide film. Abstract.
>
> It is an object of the present invention to provide a method of manufacturing a semiconductor device in which the *thickness of a first gate oxide film can be set independently of the thickness of a gate oxide film formed in a later thermal oxidation step*. Column 1, line 66-Column 2, line 2.

Thus, *Nakata* teaches that the *thickness of the first gate oxide film can be set independently of the thickness of a gate oxide film formed in a later thermal oxidation step*. The Examiner has not shown why the teaching of a method for producing a flash-EEPROM memory array and associated transistors using the DPCC process as taught in *Cappelletti* should be combined with the teaching of setting the thickness of a first gate oxide film independently of the thickness of a gate oxide film formed in a later thermal oxidation step from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *In re*

Rouffett, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must provide **objective** evidence for combining *Cappelletti* which teaches a method for producing a flash-EEPROM memory array and associated transistors using the DPCC process with *Nakata* which teaches setting the thickness of a first gate oxide film independently of the thickness of a gate oxide film formed in a later thermal oxidation step. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

As stated above, the Examiner's motivation for combining *Cappelletti* with *Nakata* is because the nitridation allows for a gate film of longer endurance. The Examiner has not shown why *Cappelletti* should be modified to include a nitridation process to allow for a gate film of longer endurance from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q. 2d 1453, 1458 (Fed. Cir. 1998). Furthermore, the Examiner has not shown why *Cappelletti* should be modified to strengthen the interface by providing a nitrification process in both the core area and the periphery area of the memory device thereby improving the reliability of the dual gate oxide in the core area from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *Id.* The Examiner must submit **objective** evidence and not rely on his own subjective opinion in support of modifying *Cappelletti* to include a nitridation process that allows for a gate film of longer endurance. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective** evidence and not rely on his own subjective opinion in support of modifying *Cappelletti* to strengthen the interface by providing a nitrification process in both the core area and periphery area ~~of the memory device thereby improving the reliability of the dual gate oxide in the~~ core area. *Id.* Therefore, the Examiner has not provided a *prima facie* case of obviousness for rejecting claims 1-4 and 10-12. Accordingly, one skilled in the art would not be able to recreate claims 1-4 and 10-12 in view of the cited prior art.

Furthermore, if the proposed modification or combination of the prior art would *change the principle of operation of the prior art invention being modified*, then the teachings of the references are not sufficient to render the claims *prima facie*

obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would *render the prior art invention being modified unsatisfactory for its intended purpose*, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). Cappelletti teaches:

> According to FIG. 10, a P-type substrate 30 has P-type wells 31; N-type wells 32; field insulating regions 34; channel stoppers 33; and a thin oxide layer 35'. As explained in more detail below *to obtain the required finish thickness of layer 35', a number of parameters are adjusted as compared with the known process described with reference to FIGS. 3-9.* As shown in FIG. 10, cell implant (EPM) mask 36 is already present, and, as in FIG. 3, a cell implant (arrows 38') is performed to obtain P-type regions 60. In view of the different characteristics of the EPROM cells formed in the process of FIGS. 3-9 and the flash-EEPROM cells formed in accordance with the present invention, the conditions of implant 38' differ from those of the EPROM process as described above. Using the same cell implant (EPM) mask 36, *gate oxide layer 35' is etched and removed from cell area 40b'*, resulting in the intermediate structure shown in FIG. 11. At this time, EPM mask 36 is removed and the wafer is cleaned. The wafer is oxidized to grow a thin oxide layer 61 directly on the surface of the substrate in cell area 40b', the oxidation parameters being selected to achieve the required characteristics, and particularly the thickness, of the thin tunnel oxide layer. *Oxidation slightly increases the thickness of the gate oxide of the circuit transistors, as shown (exaggerated for clarity) by the dotted line in FIG. 12 showing the original thickness of layer 35'. The gate oxide layer on the circuit portion is indicated as 35" to take into account the increased thickness, though it is substantially equivalent to layer 35 in the known process. As stated above, the initial thickness of gate oxide layer 35' must be calculated to allow for the increase in tunnel oxidation and the slight reduction when the wafer is cleaned prior to forming the thin tunnel oxide.* Column 4, lines 21-53.

> The process according to the present invention thus provides a method for producing *a flash-EEPROM memory array and associated transistors using the DPCC process*, and thus exploits the intrinsic advantages, and in particular the experience and know-how of the process for obtaining memories of known, reliable electric characteristics. Moreover, the possibility of producing flash-EEPROM memories using the DPCC process allows for the production of two families of products (EPROM and flash-EEPROM memories) on the

same fabrication line with no significant differences, and by using the same machinery. Column 5, lines 1-11.

Thus, Cappelletti teaches producing a flash-EEPROM memory using the DPCC process which involves forming an appropriate thickness of the gate oxide of the circuit transistors. Nakata teaches:

> Sectional views of another embodiment of the present invention are shown in FIGS. 3A to 3H. An element isolation region having an element isolation insulating film 2 and an *element region having a first oxide film 3 are formed on a semiconductor substrate 1 of a first conductivity type.* As the first oxide film 3, a film is formed by thermal oxidation at a temperature of, e.g., 800.degree. C. to 1,150.degree. C., to have a thickness of about 100 .ANG. to 400 .ANG. (FIG. 3A). Subsequently, the *first oxide film 3 is selectively etched by, e.g., hydrofluoric acid using a photoresist 4 (FIG. 3B). After the photoresist 4 is removed, a second oxide film 5 prospectively serving as a gate oxide film is formed by thermal oxidation* at a temperature of, e.g., 800.degree. C. to 1,150.degree. C. to have a thickness of about 50 .ANG. to 200 .ANG.. At this time, the *first oxide film 3 is oxidized to increase the thickness thereof, thereby obtaining a first oxide film 3a having a large thickness (FIG. 3C).* After two types of oxide films, i.e., the *first oxide film 3a having the large thickness and the second oxide film 5 are formed in the element region*, the entire surface of the resultant structure is nitrified by annealing the resultant structure in a nitrogen gas atmosphere or an ammonia gas atmosphere. *The nitrification is performed* in the nitrogen gas atmosphere at a temperature of 1,000.degree. C. to 1,200.degree. C., and the nitrification is performed in the ammonia gas atmosphere at a temperature of 900.degree. C. to 1,150.degree. C. Thermal oxidation is performed at a temperature of, e.g., 800.degree. C. to 1,150.degree. C. to uniform the properties of the first and second oxide films (FIG. 3D). A *nitrified first oxide film 6 is selectively removed* by, e.g., hydrofluoric acid, using a photoresist 8 (FIG. 3E). A *third oxide film 9 prospectively serving as a gate oxide film is formed by thermal oxidation* at a temperature of, e.g., 800.degree. C. to 1,150.degree. C., to have a thickness of about 100 .ANG. to 500 .ANG.. At this time, *the nitrified first oxide film 6 and a nitrified second oxide film 7 are rarely oxidized not to increase the thicknesses thereof* (FIG. 3F). A gate electrode 10 constituted by a polysilicon film is formed (FIG. 3G), and diffusion layers 11 prospectively serving as a source and a drain are formed. An insulating interlayer 12 is formed, contact holes 12a are formed, and wiring electrodes 13 are formed. A covering insulating film 14 is formed as a protection film (FIG. 3H). Column 3, lines 7-50.

Thus, Nakata teaches a first gate oxide whose thickness is independent of the thickness of the gate oxide film formed later in a thermal oxidation step. This may occur by having two types of oxide films which includes a first oxide film having a large thickness and a second oxide film formed in the element region. The entire surface of the structure is nitrified by annealing the structure in a nitrogen gas atmosphere or an ammonia gas atmosphere. A third oxide film may later be formed by thermal oxidation. At this time, the nitrified first oxide film and nitrified second oxide film are rarely oxidized to not increase the thickness thereof. By following these steps in the process, the nitrified first oxide film and the nitrified second oxide film form a step difference. Since the gate access films are nitrified (first oxide film and second oxide film) as explained above, the thickness of the first gate oxide film can be set independently of a gate oxide film formed by the sequential thermal oxidation. However, by combining *Nakata* with *Cappelletti, Cappeletti* would not be able to produce a flash-EEPROM memory using the DPCC process **as the thickness of the gate oxide layer would not be able to be produced with the required finish thickness by having to include the additional steps of a second oxide film formed by thermal oxidation and nitrifying both the first and the second oxide films followed by forming a third oxide film by thermal oxidation**. By including these additional steps, gate oxide layer 35' in *Cappelletti* would not be able to be formed with the appropriate thickness using the process outlined in column 4, lines 21-53 in *Cappelletti*. Hence, by combining *Cappelletti* with *Nakata*, the *principle of operation in Cappelletti would change* and subsequently *render the operation of Cappelletti to perform its purpose unsatisfactory*. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-4 and 10-12.

2. **There is no motivation to combine *Cappelletti* and *Nakata* with *Lee***

There is no motivation to combine *Cappelletti* and *Nakata* with *Lee* as there is no suggestion or motivation in either *Cappelletti*, *Nakata* or *Lee*, or in their combination, or in the knowledge of those ordinarily skilled in the art to combine the teaching of producing a flash-EEPROM memory using the DPCC process as taught in

Cappelletti with setting the thickness of a first gate oxide film independently from the thickness of the gate oxide film formed in a later thermal oxidation step as taught in *Nakata* with the teaching of simplifying the CMOS process by reducing the number of photomasks as well as optimizing the n-channel implants of the array and periphery relative to one another as taught in *Lee*. As stated above, *Cappelletti* teaches producing a flash-EEPROM memory using the DPCC process. As stated above, *Nakata* teaches setting the thickness of a first gate oxide film to be independent of the thickness of a gate oxide film formed in a later thermal oxidation step. *Lee* teaches:

> The described invention comprises a significant improvement over the prior art as such a CMOS process is now simplified and enables optimization of implants without additional process complexity. For example, the prior art requires six photomask steps as described above in the background. However in accordance with the above preferred embodiment, the *number of photomasks has been reduced to three* (that which produces FIGS. 7, followed by FIG. 8 and FIG. 12), and as well the n-*channel implants of the array and periphery can be optimized relative to one another*. With the prior art, optimization of such regions would require another photomask step, bringing the total to seven. Column 7, lines 4-16.

Thus, *Lee* teaches simplifying the CMOS process by reducing the number of photo masks required as well as optimizing the n-channel implants of the array and periphery relative to one another. The Examiner has not shown why the teaching of producing a flash-EEPROM memory from the DPCC process as taught in *Cappelletti* and the teaching of setting the thickness of a first gate oxide film independently of the thickness of a gate oxide film formed in a later thermal oxidation step as taught in *Nakata* should be combined with the teaching of simplifying the CMOS process by reducing the number of photomasks as well as optimizing the n-channel implants of the array and periphery relative to one another from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must submit **objective** evidence for combining *Cappelletti* which teaches producing a flash-EEPROM memory using a DPCC process with *Nakata* which teaches setting

the thickness of a first gate oxide film independently from the thickness of a gate oxide film formed in a later thermal oxidation step with *Lee* which teaches simplifying the CMOS process by reducing the number of photomasks and optimizing the n-channel implants of the array and periphery relative to one another. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Moreover, the Examiner states that "*Lee* discloses a conventional process for simultaneous memory and peripheral formation including *forming a polysilicon layer 24 and a ONO layer 26 and removing both of these layers from the peripheral region 10* (see Figures 2A-2B in column 3, lines 4-55) and a subsequent process to form a second polysilicon layer in the memory and peripheral areas. In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process so as to include memory and peripheral gate formation process of *Lee* in the reference of *Cappelletti et al* modified by *Nakata because this is shown to be conventional fabrication for memory and peripheral circuits*." Paper No. 8, page 3.

The Examiner has not shown why *Cappelletti* should be modified to form a polysilicon layer and a ONO layer and removing both of these layers from the peripheral region from either the nature of the problem to be solved, the teaching of the prior art or the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Further, the Examiner has not shown why *Cappelletti* should be modified to deposit a layer of type-1 polysilicon in both the core area and periphery area of the memory device, to deposit a layer of oxide nitride oxide over the layer of type-1 polysilicon and to remove the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device from either the nature of the problem to be solved, the teaching of the prior art or the knowledge of persons of ordinary skill in the art. *Id.* The Examiner must submit **objective** evidence and not rely on his own subjective opinion in support of modifying *Cappelletti* to form a polysilicon layer and a ONO layer and removing both of these layers from the peripheral region. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective** evidence

and not rely on his own subjective opinion in support of modifying *Cappelletti* to deposit a layer of type-1 polysilicon in both the core area and periphery area of the memory device, to deposit a layer of oxide nitride oxide over the layer of type-1 polysilicon and to remove the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device. *Id.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2 and 10. Accordingly, one skilled in the art would not be able to recreate claims 2 and 10 in view of the cited prior art.

C. *Cappelletti, Nakata*, and *Lee* taken singly or in combination, do not teach or suggest the following claim limitations.

Cappelletti, *Nakata* and *Lee*, taken singly or in combination, do not teach or suggest "simultaneously providing a *dual gate oxide* in a *core area of the memory device* and *completing the dual gate oxide of the periphery area*, wherein the *dual gate oxide in the core area forms an interface between the oxide and the silicon substrate*" as recited in claims 1 and 10. The Examiner states "*Nakata* shows in Figures 3C and 3D, simultaneously nitrifying oxide regions 6 and 7 of different thicknesses. Furthermore, *Nakata* states at column 3, lines 51-58 that these nitride films can be formed at different element regions to form different types of MOS transistors with different thicknesses. Clearly, this provides ample motivation to combine the references of *Cappelletti, et al* with *Nakata* as stated in the rejection under 35 USC 103 above." Paper No. 8, page 4. Applicants respectfully assert that the Examiner has not provided any **objective** evidence for modifying *Cappelletti* with *Nakata* to nitrify oxide regions of different thickness'. *In re Lee*, 61 U.S.P.Q 2d 1430, 1434 (Fed. Cir. 2002). Further, *Nakata* teaches:

> In this embodiment, a MOS transistor having a first gate insulating film in which the *nitrified first oxide film 6 and the nitrified second oxide film 7 forms a step difference is formed.* However, when these nitrified oxide films are respectively formed in different element regions, three types of MOS transistors having different gate insulating films can be integrated on the same silicon substrate. Column 3, lines 51-58.

Thus, *Nakata* teaches nitrified oxide films of different thickness'. However, this language does not teach or suggest *simultaneously providing* a dual gate oxide in a core area of the memory device and *completing* the dual gate oxide in the periphery area. Further, *Nakata* teaches a *nitrified first oxide film 6 and a nitrified second oxide film 7 being formed in the element region.* Thus, *Nakata* does not teach *simultaneously providing a dual gate oxide* in a *core area of the memory device* and *completing the dual gate oxide* in the *periphery area.* Accordingly, one skilled in the art would not be able to recreate claims 1 and 10 in view of the cited art.

Cappelletti, *Nakata* and *Lee*, do not teach or suggest "*strengthening the interface* by providing a nitrification process *in both the core area and the periphery area of the memory device subsequent to steps (a) and (b), thereby improving the reliability of the dual gate oxide in the core area*" as recited in claims 1 and 10. The Examiner directs Applicants attention to column 3, lines 51-58 of *Nakata* as teaching the above-cited claim limitation. Paper No. 8, page 2. Instead, as stated above, *Nakata* teaches forming nitrified oxide films with a step difference between them in an element region on a semiconductor substrate. This language does not teach or suggest *strengthening the interface* by providing a nitrification process in *both the core area and periphery area of the memory device.* Furthermore, this language does not teach or suggest strengthening the interface by providing a nitrification process in both the core area and the periphery area of the memory device *subsequent to steps (a) and (b).* Further, *Nakata* teaches:

> After two types of oxide films, i.e., the *first oxide film 3a having the large thickness and the second oxide film 5 are formed in the element region, the entire surface of the resultant structure is nitrified by annealing the resultant structure in a nitrogen gas atmosphere or an ammonia gas atmosphere.* The nitrification is performed in the nitrogen gas atmosphere at a temperature of 1,000.degree. C. to 1,200.degree. C., and the nitrification is performed in the ammonia gas atmosphere at a temperature of 900.degree. C. to 1,150.degree. C. *Thermal oxidation is performed at a temperature of, e.g., 800.degree. C. to 1,150.degree. C. to uniform the properties of the first and second oxide films (FIG. 3D).* A nitrified first oxide film 6 is selectively removed by, e.g., hydrofluoric acid, using a photoresist 8 (FIG. 3E). *A third oxide film 9 prospectively serving as a gate oxide film is formed*

> *by thermal oxidation* at a temperature of, e.g., 800.degree. C. to 1,150.degree. C., to have a thickness of about 100 .ANG. to 500 .ANG.. At this time, the nitrified first oxide film 6 and a nitrified second oxide film 7 are rarely oxidized not to increase the thicknesses thereof (FIG. 3F). A gate electrode 10 constituted by a polysilicon film is formed (FIG. 3G), and diffusion layers 11 prospectively serving as a source and a drain are formed. An insulating interlayer 12 is formed, contact holes 12a are formed, and wiring electrodes 13 are formed. A covering insulating film 14 is formed as a protection film (FIG. 3H). Column 3, lines 24-50.

Thus, *Nakata* teaches *nitrifying the oxide films in the element region prior to performing a thermal oxidation of the first and second oxide films and forming a third oxide film on the element isolation region.* Furthermore, this language does not teach or suggest strengthening the interface by providing a nitrification process to both the core area and the periphery area of the memory device subsequent to steps (a) and (b), thereby *improving the reliability of the dual gate oxide in the core area.* Instead, *Nakata* teaches that "it is another object of the present invention to provide a method of manufacturing a semiconductor device capable of *decreasing variations in thickness of a gate oxide film.*" Column 2, lines 3-6. Nakata further teaches that "at this time, the nitrified first oxide film 6 and a nitrified second oxide film 7 are rarely oxidized not to increase the thicknesses thereof (FIG. 3F)." Column 3, lines 41-44. Thus, *Nakata* teaches *nitrifying the oxide films in the element region to decrease the variation and thickness of the oxide films and not to improve the reliability of the dual gate oxide in the core area.* Accordingly, one skilled in the art would not be able to recreate claims 1 and 10 in view of the cited prior art.

Cappelletti, *Nakata*, *Lee* and *Chien*, taken singly or in combination, do not teach or suggest "depositing a layer of type-1 polysilicon in both the core area and periphery area of the memory device; depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon; and removing the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device" as recited in claim 10. The Examiner directs Applicants' attention to Figures 2A-2B and column 3, lines 4-55 of *Lee* as teaching the above-cited claim limitation. Paper No. 8, page 3. Instead, *Lee* teaches:

> Prior art techniques of processing erasable PROMs are described with reference to FIGS. 1A-5. FIG. 1A is a top view of a wafer fragment at one processing step, with FIG. 1B being an enlarged cross section taken through line 1B--1B of FIG. 1 during the same step. In each of the figures which follow, the "A" figure represents a top view, while the "B" view represents an enlarged cross sectional view at the same step in the described process. FIGS. 1A and 1B illustrate a wafer fragment 10 which will be defined by a memory array area 12 and an area 14 peripheral to array area 12. Wafer fragment 10 is comprised of a bulk substrate 16, which in the described embodiment is p-type, with peripheral area 14 being provided with n-well 18 for formation of CMOS transistors in the peripheral area 14. Field oxide regions 20 and a gate insulating layer 22 are provided atop substrate 16. *A first layer 24 of polysilicon (Poly 1) is applied atop insulating layers 20 and 22.* A *tri-layer 26 of dielectric is applied atop first polysilicon layer 24 for use in floating gate transistors to be formed within array area 12.* Tri-layer 26 typically comprises an O--N--O sandwich construction. Referring to FIGS. 2A and 2B, *dielectric layer 26 and polysilicon layer 24 are etched away from peripheral area 14, and etched within array 12 to define lines 28.* Lines 28 are defined by opposing edges 30a and 30b which will form the first two edges of the floating gate transistors within array 12, as will be apparent from the continuing discussion. Column 3, lines 4-32.

Thus, *Lee* teaches applying a first layer 24 of poly 1 atop insulating layers 20 and 22. *Lee* further teaches applying a dielectric layer 26 atop polysilicon layer 24. *Lee* further teaches etching dielectric layer 26, polysilicon layer 24 from peripheral area 14. This language does not teach or suggest *removing a portion of the layer of polysilicon layer 24 from the peripheral area* as illustrated in Figure 2B of *Lee*. Accordingly, one skilled in the art would not be able to recreate claim 10 in view of the cited prior art.

For at least the above reasons, claims 1 and 10 are patentable over *Cappelletti* in view of *Nakata* and further in view of *Lee* and further in view of *Chien*. Claims 2-4 and 11-12 each recite combinations of features including the above combinations, and thus are patentable for at least the above reasons as well. Claims 2-4 and 11-12 recite additional features which, in combination with the features of the claims upon which they depend, are patentable over *Cappelletti* in view of *Nakata* and further in view of *Lee* and further in view of *Chien*.

For example, *Cappelletti*, *Nakata* and *Lee*, taken singly or in combination, do not teach or suggest "(d) depositing a layer of type-1 polysilicon of both the core area and the periphery area of the memory device; (e) depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon; and (f) *removing* the layer of oxide nitride oxide and a *portion of the layer of type-1 polysilicon from the periphery area of the memory device*" as recited in claim 2. For at least the above stated reasons, *Cappelletti*, *Nakata* and *Lee* do not teach or suggest the above-cited claim limitations. Accordingly, one skilled in the art would not be able to recreate claim 2 in view of the cited prior art.

D. The rejections of claims 3-4 and 11-12 are moot on the ground that *Chien* is not a prior art reference.

Applicants respectfully submit that *Chien* is not a prior art reference because *Chien*'s filing date post dates the filing date of the present invention. The present invention is a divisional application of a parent application filed June 15, 2000. *Chien*'s filing date is January 19, 2001. Accordingly, *Chien* cannot be a prior art reference in the present invention. Therefore, the rejections of claims 3-4 and 11-12 are moot.

E. Conclusion.

As a result of the foregoing, Applicants respectfully assert that the Examiner's *prima facie* case of obviousness is not taught or suggested by the cited prior art since there are numerous claim limitations not taught or suggested in the cited prior art, and thus one skilled in the art would not have been able recreate claims 1-4 and 10-12 in view of the cited prior art.

It is noted that words are italicized only for emphasis. Words that are italicized are not meant to imply that only those words are not taught or suggested in the cited prior art.

II. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-4 and 10-12 in the application are in condition for allowance, and respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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